I, Tadahiko Itoh, a Patent Attorney of Tokyo, Japan having my office at 32nd Floor, Yebisu Garden Place Tower, 20-3 Ebisu 4-Chome, Shibuya-Ku, Tokyo 150-6032, Japan do solemnly and sincerely declare that I am the translator of the attached English language translation and certify that the attached English language translation is a correct, true and faithful translation of Japanese Patent Application No. 2003-100170 to the best of my knowledge and belief.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(Document Name)	Application for Patent
(Reference Number)	JPP030031
(Destination)	Commissioner of Patent Office
(IPC)	H01L 21/00
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(Prepayment Ledger Number)	058171
(Amount Paid)	¥ 21,000
(List of Submitted Documents)	
(Document Name)	Specification 1
(Document Name)	Drawing 1
(Document Name)	Abstract 1
(Proof Requested or not)	Requested

[Document Name] DESCRIPTION

[Title of Invention] SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

[Claims]

[claim 1]

A semiconductor device comprising:

a silicon substrate;

a gate electrode layer; and

a gate insulation film disposed between the silicon substrate and the gate electrode layer,

wherein

the gate insulation film is a high relative permittivity (high-k) film being formed by performing a nitriding treatment on a mixture of a metal and silicon.

[claim 2]

The semiconductor device as claimed in claim 1, wherein the gate insulation film is formed according to a plasma CVD technology.

[claim 3]

The semiconductor device as claimed in claim 1 or 2, wherein a silicon nitride film is formed as a barrier layer between the silicon substrate and the gate insulation film.

[claim 4]

The semiconductor device as claimed in claim 3, wherein the silicon nitride film is formed according to a direct nitriding technology by plasma.

[claim 5]

The semiconductor device as claimed in claim 1, 2, 3, or 4, wherein a silicon nitride film is disposed on the gate insulation film.

[claim 6]

The semiconductor device as claimed in claim 5, wherein the silicon nitride film and the gate insulation film are

alternately laminated on the silicon substrate.

[claim 7]

The semiconductor device as claimed in claim 1 or 2, wherein a buffer layer is formed between the silicon substrate and the gate insulation film.

[claim 8]

The semiconductor device as claimed in claim 1 or 2, wherein an alumina (Al_2O_3) monocrystal film is formed between the silicon substrate and the gate insulation film.

[claim 9]

The semiconductor device as claimed in claim 8, wherein the alumina monocrystal film is formed according to a plasma CVD technology.

[claim 10]

The semiconductor device as claimed in claim 1, 2, 3, 4, 5, 6, 7, 8, or 9, wherein the gate insulation film has one of compositions selected from a following list:

$M_3Si_6N_{11}$ (M=La, Ce, Pr, Nd, Sm);

$M_2Si_5N_8$ (M=Ca, Sr, Ba, Eu);

$MYbSi_4M_7$ (M=Sr, Ba, Eu);

$BaSi_4N_7$;

$Ba_2Nd_7Si_{11}N_{23}$.

[claim 11]

A method for manufacturing a semiconductor device comprising the steps of:

forming a gate insulation film which is a high relative permittivity (high-k) film by performing a nitriding treatment on a mixture of a metal and silicon; and

forming a gate electrode layer on the gate insulation film.

[claim 12]

The method for manufacturing the semiconductor device as claimed in claim 11, wherein the gate insulation film is

formed according to a plasma CVD technology.

[claim 13]

The method for manufacturing the semiconductor device as claimed in claim 11 or 12, further comprising the step of forming a silicon nitride film as a barrier layer between the silicon substrate and the gate insulation film.

[claim 14]

The method for manufacturing the semiconductor device as claimed in claim 13, wherein the silicon nitride film is formed according to a direct nitriding by plasma.

[claim 15]

The method for manufacturing the semiconductor device as claimed in claim 11, 12, 13, or 14, wherein a silicon nitride film is disposed on the gate insulation film.

[claim 16]

The method for manufacturing the semiconductor device as claimed in claim 15, wherein the silicon nitride film and the gate insulation film are alternately laminated on the silicon substrate.

[claim 17]

The method for manufacturing the semiconductor device as claimed in claim 11 or 12, further comprising the step of forming a buffer layer between the silicon substrate and the gate insulation film.

[claim 18]

The method for manufacturing the semiconductor device as claimed in claim 11 or 12, further comprising the step of forming an alumina (Al_2O_3) monocrystal film between the silicon substrate and the gate insulation film.

[claim 19]

The method for manufacturing the semiconductor device as claimed in claim 18, wherein the alumina monocrystal film is formed according to a plasma CVD technology.

[claim 20]

The method for manufacturing the semiconductor device as claimed in claim 11, 12, 13, 14, 15, 16, 17, 18, or 19, wherein the gate insulation film has one of compositions selected from a following list:

$M_3Si_6N_{11}$ (M=La, Ce, Pr, Nd, Sm);

$M_2Si_5N_8$ (M=Ca, Sr, Ba, Eu);

$MYbSi_4N_7$ (M=Sr, Ba, Eu);

$BaSi_4N_7$;

$Ba_2Nd_7Si_{11}N_{23}$.

[Detailed Description of the Invention]

[0001]

[Technical Field]

The present invention generally relates to an improvement of a semiconductor device in which a high relative permittivity (high-k) film is used as a gate insulation film.

[0002]

[Background Art]

In the conventional technology, polysilicon (Poly-Si) is mainly used as an electrode material which is formed on a silicon substrate. As a gate insulation film provided between the silicon substrate and the polysilicon electrode material, a silicon oxide (SiO_2), a silicon oxynitride (SiON), and a silicon nitride (Si_3N_4) are used. As a related matter, in order to increase the capacity (proportional to ε/d, where ε is relative permittivity, and d is film thickness) of the gate insulation film, the thickness of the gate insulation film (SiO_2 (ε=3.9)) is conventionally reduced.

[0003]

According to Japanese Laid-Open Patent Application No. 2000-294550, a method is disclosed wherein

a gate insulation film having an equivalent oxide thickness of 1 nm or less is provided by performing an oxidation, nitriding, and oxynitriding directly on the surface of the wafer W by plasma processing.

[0004]

There is a limitation to reducing the thickness of the gate insulation film; however, a method is presently suggested wherein the physical thickness of the layer can be increased to a certain extent by using a material having a high relative permittivity (High-K, where K is an equivalent to ε).

[0005]

[Patent Document 1] Patent Laid-Open Publication No. 2000-294550

[0006]

[Problem to be solved by the Invention]

A conventional High-K film is made from oxide; however, oxidizing species are indispensable when forming an oxide film. Further, it is necessary to perform a high heating treatment in an atmosphere of the oxidizing species or inert gas species so as to stabilize the crystallinity of the oxide. As a result, SiO_2 (or a metal mixture including Si, O, and a High-K material) is formed on the Si surface or on the surface of the oxide High-K film. Accordingly, layers having a low relative permittivity are formed serially. Therefore, the original object of increasing the capacity cannot be achieved.

[0007]

Accordingly, a method is suggested for providing a silicon nitride film (ε is about 7) between the Si surface and High-K material so as to prevent the SiO_2 film from being formed. However, the silicon nitride film is oxidized while the High-K film is formed. Thus, it is difficult to form

only a film having a high relative permittivity.

[0008]

The present invention was made in consideration of the above described problems. It is a general object of the present invention to provide a semiconductor device having good quality by keeping the relative permittivity of a High-K insulation film in a high state. Another object of the present invention is to provide a method for manufacturing a semiconductor device in which the relative permittivity of the High-K insulation film can be kept in a high state.

[0009]

[Means of Solving the Problem]

In order to achieve the above described objects, a semiconductor device is provided including a silicon substrate, a gate electrode layer, and a gate insulation film between the silicon substrate and the gate electrode layer. The gate insulation film is a high relative permittivity (high-k) film being formed by performing a nitriding treatment on a mixture of a metal and silicon. In other words, the High-K film itself is a nitride so as to prevent SiO_2 from being formed.

[0010]

As for the above described gate insulation film, it is preferable to form the film according to a plasma CVD technology. Further, in a case where a silicon nitride film is provided as a barrier layer between the silicon substrate and the gate insulation film, it is less likely that the thickness of the film increases while the High-K material is being formed. Thus, a decrease of the capacity can be controlled. This is based on the fact that the thickness of the silicon nitride film is less likely to increase than the thickness of the oxide film. It should be noted that

the above described silicon nitride layer can be formed according to a direct nitriding by plasma processing.

[0011]

Moreover, a silicon nitride film is provided on the gate insulation film so as to control a reaction with the gate electrode.

[0012]

Furthermore, a more stable insulation film can be obtained by laminating the silicon nitride films and the gate insulation films alternately on the silicon substrate.

[0013]

Further, interfacial quality can be improved and a good FET quality can be obtained by forming a buffer layer between the silicon substrate and the gate insulation film.

[0014]

In addition, the relative permittivity of the buffer layer can be increased to substantially 9 by forming an Alumina (Al_2O_3) monocrystal film between the silicon substrate and the gate insulation film. Accordingly, the capacity can be further increased. It should be noted that the above described alumina monocrystal film can be formed according to the plasma CVD technology.

[0015]

As for the above described gate insulation film, one of the following compositions can be adopted:

$M_3Si_6N_{11}$ (M=La, Ce, Pr, Nd, Sm);

$M_2Si_5N_8$ (M=Ca, Sr, Ba, Eu);

$MYbSi_4N_7$ (M=Sr, Ba, Eu);

$BaSi_4N_7$;

$Ba_2Nd_7Si_{11}N_{23}$.

[0016]

[Best Mode for Carrying out the Invention]

Fig.1 is a schematic diagram showing an example

of the configuration of a plasma treatment apparatus 10 according to the present invention. The plasma treatment apparatus 10 includes a treatment container 11 in which a substrate holding board 12 retaining a silicon wafer W as a substrate to be treated is embedded. Gas in the treatment container 11 is exhausted from exhaust ports 11A and 11B via an exhaust pump of which a drawing is omitted. It should be noted that the substrate holding board 12 has a function of heating the silicon wafer W. In the periphery of the substrate holding board 12, a gas baffle plate (partition) 26 which includes aluminum is provided. On the upper side of the gas baffle plate 26, a quartz cover 28 or a SiC cover 28 is provided.

[0017]

On the upper side of the treatment container 11, an open part corresponding to the silicon wafer W on the substrate holding board 12 is provided. The above open part is closed by a dielectric board 13 which includes quartz, Al_2O_3, AlN, and Si_3N_4. On the upper side of the dielectric board 13, (outside of the treatment container 11) a plane antenna 14 is disposed. On the plane antenna 14, plural slots are provided so that an electromagnetic wave which is supplied from a wave guide 18 can permeate via the slots. On the further upper side (outside) of the plane antenna 14, a wavelength shortening board 15 and the wave guide 18 are provided. On the outside of the treatment container 11, a cooling plate 16 is disposed so as to cover the upper side of the wavelength shortening board 15. In the cooling plate 16, a coolant path 16a in which a coolant flows is provided.

[0018]

On the side wall of the inside of the treatment container 11, a gas feed opening 22 is provided for introducing a gas when performing a plasma treatment. A

separate gas feed opening 22 can be provided for each gas to be introduced. In this case, a mass flow controller of which the drawing is omitted is provided as means for flow control on each gas feed opening 22. As a related matter, a gas feed opening 22 can be a nozzle to which gases to be introduced being mixed in advance are supplied. In this case, the flow of the gas to be introduced is controlled by a flow regulating valve in the step of mixing the gas.

Moreover, in the inside of the wall of the treatment container 11, a coolant flow path 24 is provided so as to surround the treatment container 11.

[0019]

The plasma treatment apparatus 10 used in the present invention embeds an electromagnetic wave generator generating a few GHz electromagnetic wave for exciting plasma, of which a drawing is omitted. The microwave generated by the electromagnetic wave generator propagates through the wave guide 15 and is introduced into the treatment container 11.

[0020]

Fig.2 is a cross section of a configuration of a semiconductor device (MISFET) according to the present invention. The present invention relates to the composition and the configuration of a gate insulation film 50. A description of each embodiment is given below. Fig.2 shows a silicon substrate 100, the gate insulation film 50, a gate electrode 52, a source/drain layer (diffusion layer) 54, and a sidewall 56.

[0021]

With reference to Figs.3 through 8, a description is given of the configuration of the gate insulation film according to the first through fifth embodiments of the present invention. It should be noted

that each figure substantially corresponds to the dash line part of Fig.2.

[0022]

Fig.3 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the first embodiment of the present invention. In the semiconductor device of the present embodiment, a nitride High-K film 104 is formed as a gate insulation film (50) on the silicon substrate 100. A silicon nitride film (Si_3N_4 layer) 102 is formed between the silicon substrate 100 and the High-K film 104. Further, a TaN layer 106 is formed as a gate electrode (52) on the High-K film 104 by spattering. The High-K film 104 is formed by using the plasma treatment device 10 according to a plasma CVD technology. The silicon nitride film 102 is formed in the same way by using the plasma treatment apparatus 10 according to a direct radical nitriding treatment. The silicon nitride film 102 performs a function of lowering the interface state.

[0023]

As the High-K film 104, for example, one of the following compositions can be adopted:

$M_3Si_6N_{11}$ (M=La, Ce, Pr, Nd, Sm);

$M_2Si_5N_8$ (M=Ca, Sr, Ba, Eu);

$MYbSi_4N_7$ (M=Sr, Ba, Eu);

$BaSi_4N_7$;

$Ba_2Nd_7Si_{11}N_{23}$.

[0024]

When forming a configuration according to the first embodiment using the plasma treatment apparatus 10 shown in Fig.1, first, the silicon substrate 100 on which a plasma treatment is to be performed is introduced into the treatment container 11 and set on the substrate holding board

12. Then, the gas in the treatment container 11 is exhausted via the exhaust ports 11A and 11B so that the inside of the treatment container 11 can be set at a predetermined treatment pressure. Next, a nitrogen gas and an inert gas are introduced into the treatment container 11 from the gas feed opening 22.

[0025]

The microwave having a few GHz generated by the electromagnetic wave generator is supplied to the treatment container 11 via the wave guide 15. The microwave is introduced into the treatment container 11 via the plane antenna 14 and the dielectric board 13. The microwave excites the plasma, and thus a nitride radical is generated. The temperature of the wafer is less than 500 ℃ when performing a plasma treatment thereon by using the plasma as above generated. The high density plasma which is generated by the microwave in the treatment container 11 forms a nitride film Si_3N_4 on the surface of the silicon substrate 100.

[0026]

The silicon substrate 100 on which the Si_3N_4 film 102 is formed is taken out of the treatment container 11. After the silicon substrate 100 is taken out, when forming a High-K film 104, the silicon substrate 100 is set in the treatment container 11 again, and the nitride film 104 is formed according to the well-known CVD technology.

[0027]

Fig.4 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the second embodiment of the present invention. In Fig.4, the same or the corresponding components of Fig.3 are allocated the same reference numbers, and overlapping descriptions are omitted. In the

configuration according to the present embodiment, in the same way as the above described first embodiment, Si_3N_4 layer 102a is formed between the High-K film 104 and the silicon substrate 100, and Si_3N_4 layer 102b is formed between the High-K film 104 and the TaN layer 106. Accordingly, reactivity with the gate electrode (TaN layer 106) is controlled and a stable layer can be formed.

[0028]

Fig.5 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the third embodiment of the present invention. In Fig.5, the same or the corresponding components of Fig.3 and Fig.4 are allocated the same reference numbers, and overlapping descriptions are omitted. In the configuration of the present embodiment, the High-K film 104 is formed between the silicon substrate 100 and the gate electrode layer (TaN layer); however, another layer such as a Si_3N_4 layer is not formed between the silicon substrate 100 and the High-K film 104 or between the High-K film 104 and the TaN layer 106.

[0029]

Fig.6 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the fourth embodiment of the present invention. In Fig.6, the same or the corresponding components of Fig.3 through Fig.5 are allocated the same reference numbers, and overlapping descriptions are omitted. In the configuration of the present embodiment, a buffer layer 110 is formed between the silicon substrate 100 and the High-K film 104. It should be noted, however, that another layer such as a Si_3N_4 layer is not provided between the High-K film 104 and the TaN layer 106.

[0030]

The buffer layer 110 is formed by changing the composition of the gas which is supplied to the treatment container 11 in the same process of forming the High-K film 104. The buffer layer 110 has the benefit of a relative permittivity higher than that of the Si_3N_4 layer, and an interface state which can be lowered.

[0031]

Fig.7 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the fifth embodiment of the present invention. In Fig.7, the same or the corresponding components of Fig.3 through Fig.6 are allocated the same reference numbers, and overlapping descriptions are omitted. In the configuration of the present embodiment, three Si_3N_4 layers 102a, 102b, and 102c and two High-K films 104a and 104b are alternately laminated on the silicon substrate 100. Accordingly, a more stable insulation film can be obtained.

[0032]

Fig.8 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the sixth embodiment of the present invention. In Fig.8, the same or the corresponding components of Fig.3 through Fig.6 are allocated the same reference numbers, and overlapping descriptions are omitted. In the configuration of the present embodiment, an alumina (Al_2O_3) monocrystal film 114 having a relative permittivity higher than that of Si_3N_4 is formed between the silicon substrate 100 and the High-K film 104. The alumina (Al_2O_3) monocrystal film 114 can be formed by using the apparatus shown in Fig.1 according to the plasma CVD technology.

[0033]

Further, the best mode for carrying out the invention and the embodiments are described based on some

examples. The present invention is not limited to these embodiments, but variations and modifications may be made without departing from the scope of the present invention.

[0034]

[Brief Description of the Drawings]

[Fig.1] Fig.1 is a schematic diagram (cross section) showing an example of the configuration of the plasma treatment apparatus according to the present invention.

[Fig.2] Fig.2 is a cross section showing the configuration of the semiconductor device according to the present invention.

[Fig.3] Fig.3 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the first embodiment of the present invention.

[Fig.4] Fig.4 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the second embodiment of the present invention.

[Fig.5] Fig.5 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the third embodiment of the present invention.

[Fig.6] Fig.6 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the third embodiment of the present invention.

[Fig.7] Fig.7 is a schematic diagram showing the configuration of the substantial part of the semiconductor device according to the fourth embodiment of the present invention.

[Fig.8] Fig.8 is a schematic diagram showing the configuration of the substantial part of the semiconductor

device according to the fifth embodiment of the present invention.

[Description of the Reference Marks]

10 plasma treatment apparatus

11 treatment container

18 wave guide

22 gas feed opening

100 silicon substrate

102 Si3N4 film

104 silicon nitride film

106 TaN layer

114 Al2O3 film

[Document Name]

[Abstract]

[Problem] The present invention provides a semiconductor device having good quality by keeping the relative permittivity of a High-K insulation film in a high state. In addition, the present invention provides a method for manufacturing a semiconductor device in which the relative permittivity of the High-K insulation film can be kept in a high state.

[Means of solving] In order to provide a semiconductor device having good quality by keeping the relative permittivity of a High-K insulation film in a high state, or to provide a method for manufacturing a semiconductor device in which the relative permittivity of the High-K insulation film can be kept in a high state, a semiconductor device is disclosed that includes a silicon substrate, a gate electrode layer, and a gate insulation film between the silicon substrate and the gate electrode layer. The gate insulation film is a high relative permittivity (high-k) film being formed by performing a nitriding treatment on a mixture of a metal and silicon. The High-K film itself

becomes a nitride so as to prevent SiO_2 from being formed.
[Selected Drawing] Fig.1

FIG.1

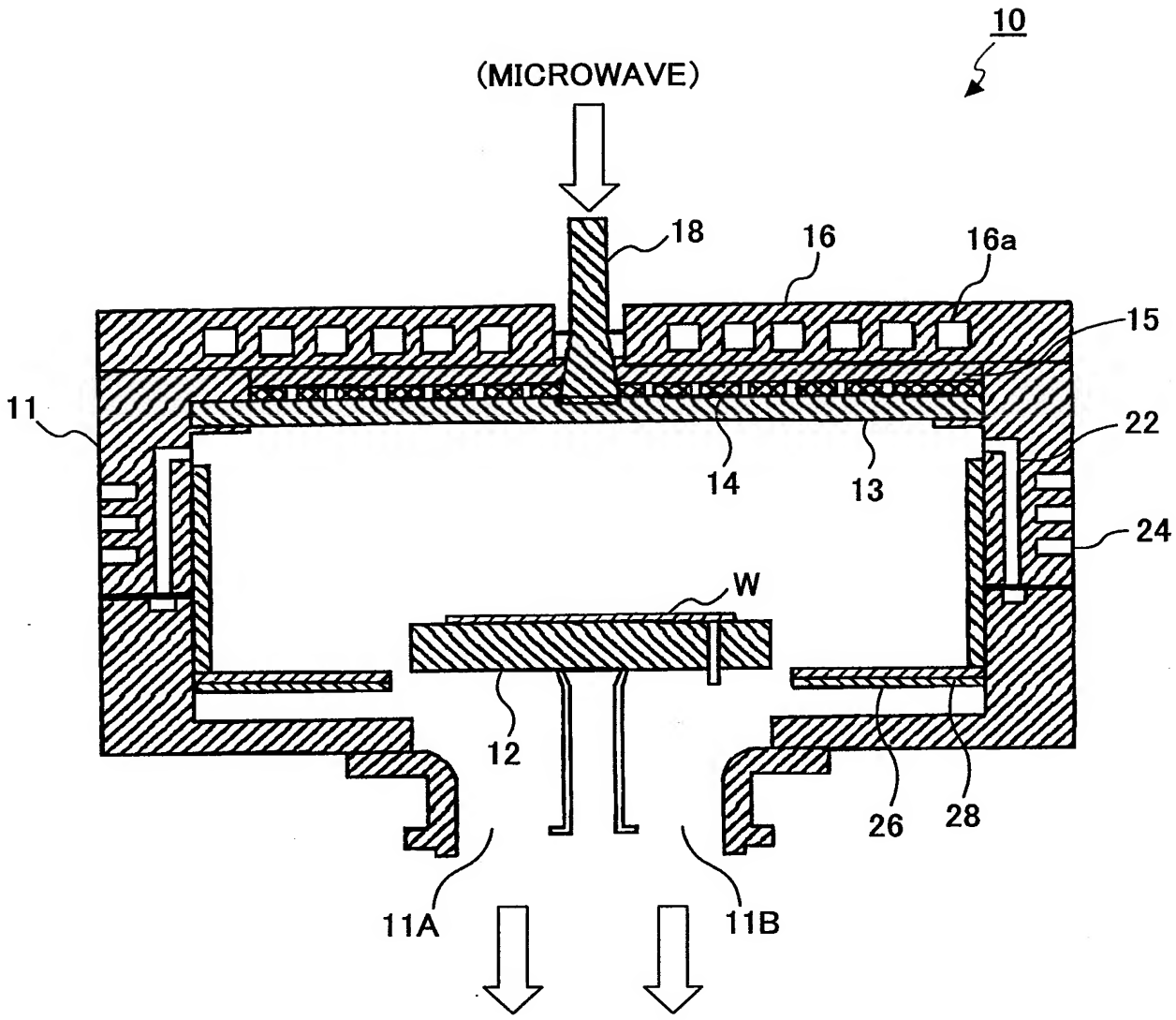


FIG.2

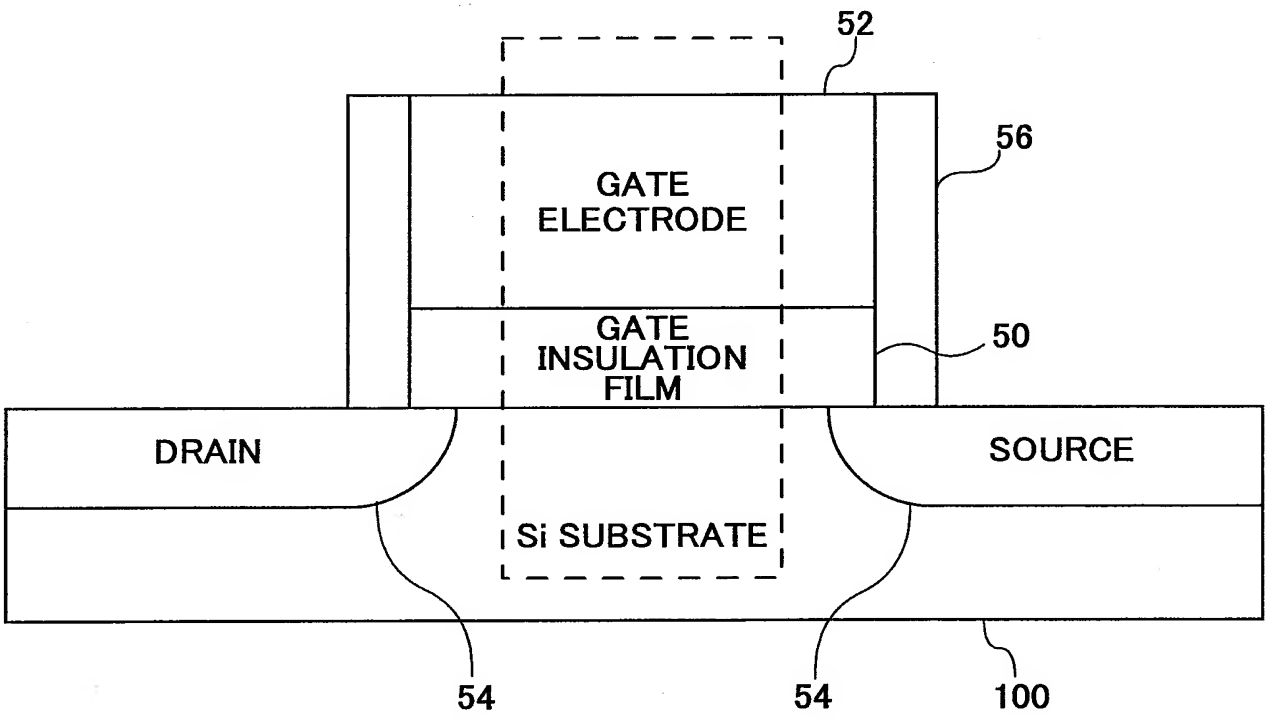

52
56
GATE ELECTRODE
GATE INSULATION FILM
50
DRAIN
SOURCE
Si SUBSTRATE
54
54
100

FIG.3

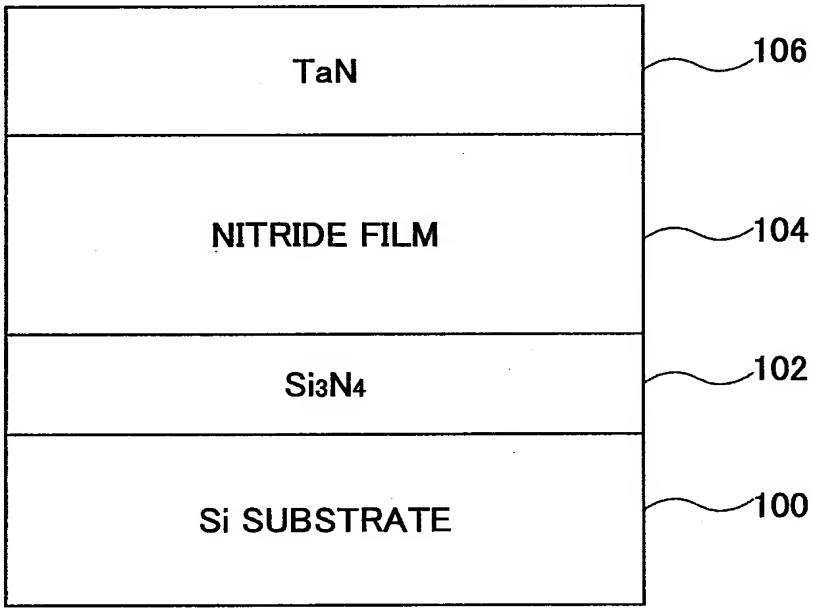

TaN
106
NITRIDE FILM
104
Si3N4
102
Si SUBSTRATE
100

FIG.4

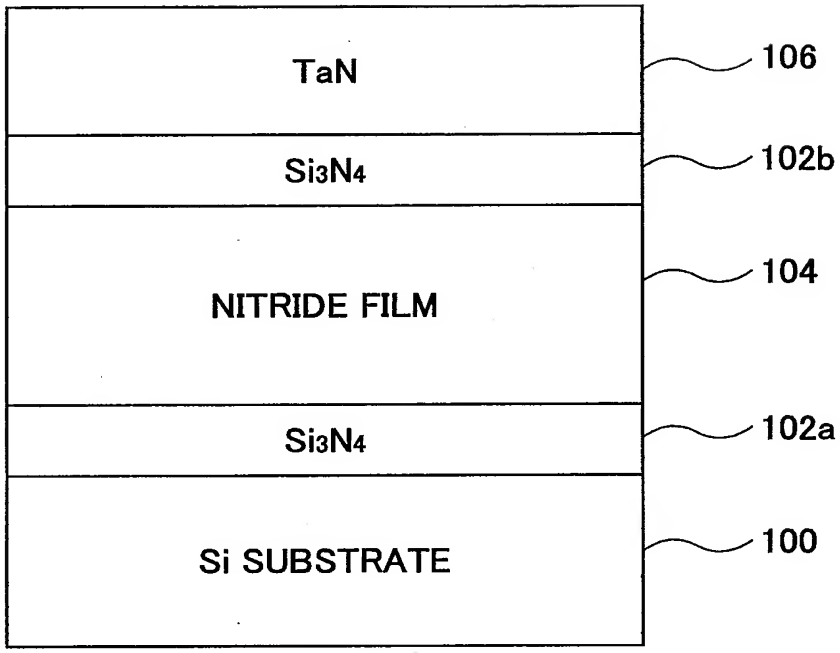

TaN
106
Si3N4
102b
NITRIDE FILM
104
Si3N4
102a
Si SUBSTRATE
100

FIG.5

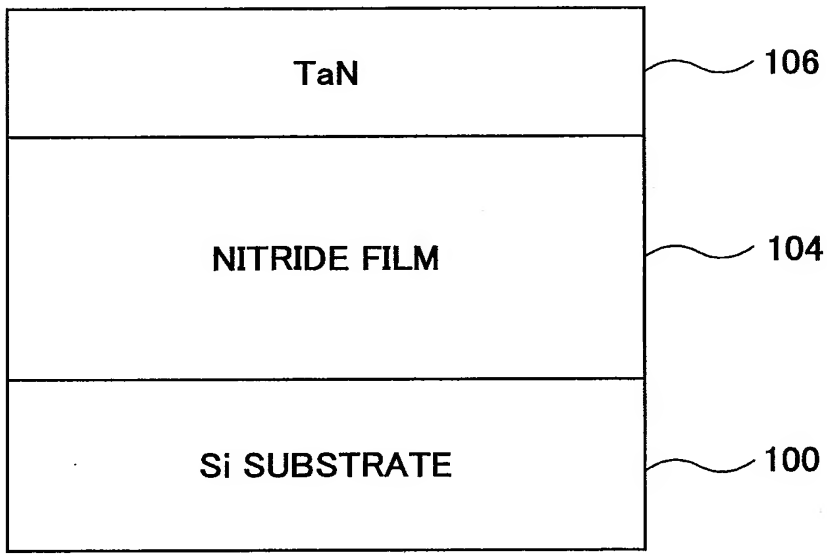

TaN
106
NITRIDE FILM
104
Si SUBSTRATE
100

FIG.6

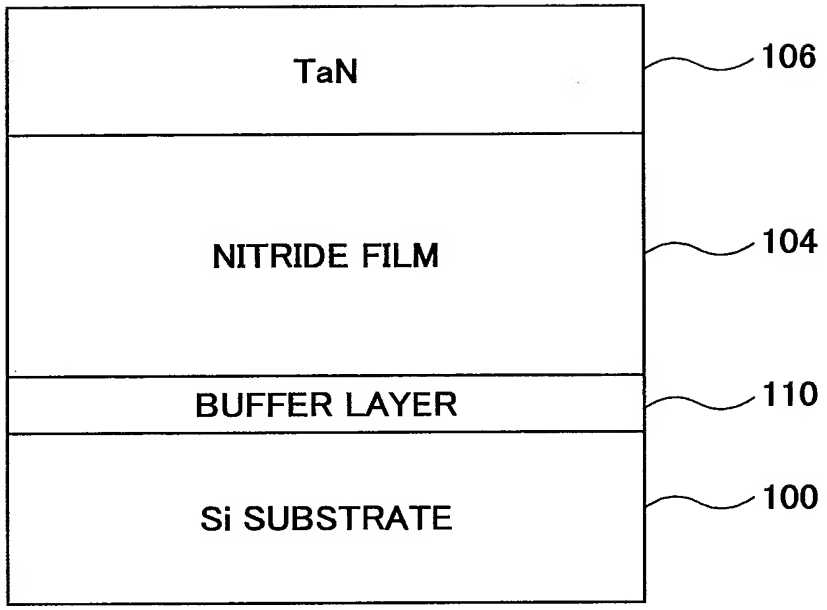

TaN
106
NITRIDE FILM
104
BUFFER LAYER
110
Si SUBSTRATE
100

FIG.7

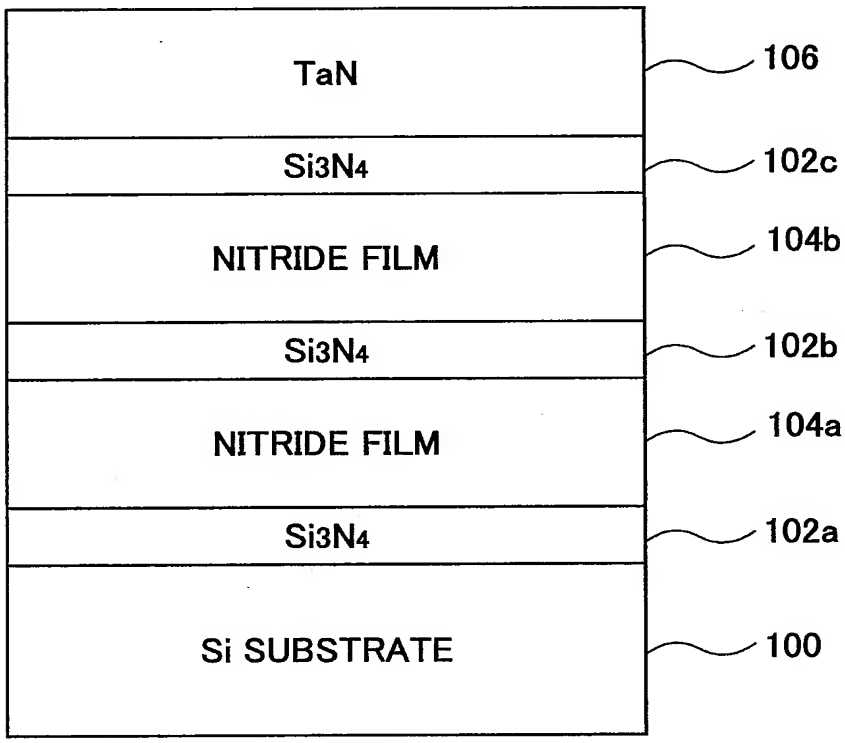
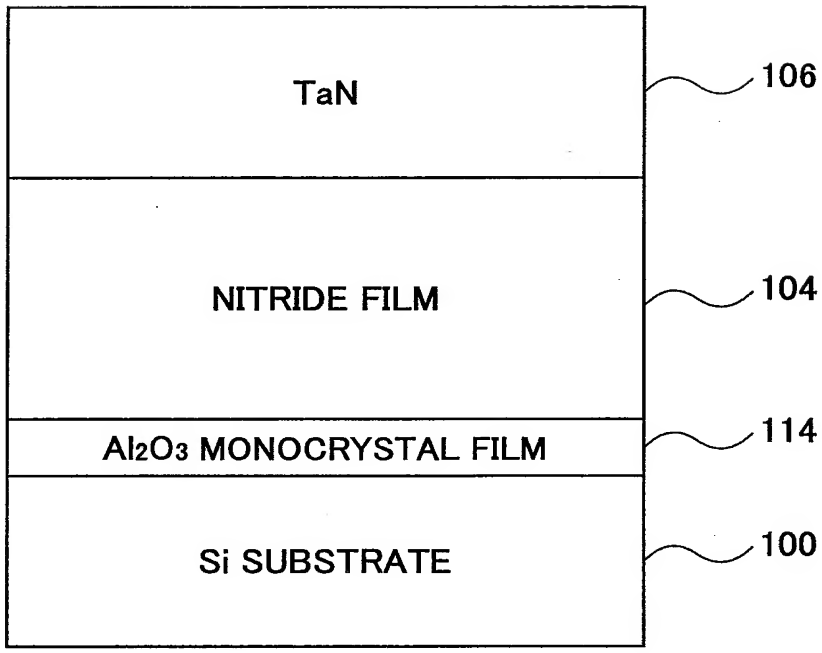

TaN
106
Si3N4
102c
NITRIDE FILM
104b
Si3N4
102b
NITRIDE FILM
104a
Si3N4
102a
Si SUBSTRATE
100

FIG.8


TaN
106
NITRIDE FILM
104
Al2O3 MONOCRYSTAL FILM
114
Si SUBSTRATE
100